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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,248	12/21/2001	Gabriel Li	CYPR-CD01080	6639

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EXAMINER	
DANG, KHANH NMN	
ART UNIT	**PAPER NUMBER**
2111	4

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,248	LI, GABRIEL	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "phase aligner" (claim 4), "encoder" (claim 4), and "serializer" (claim 4); a "deserializer" (claim 5), "framer" (claim 5), "decoder" (claim 5), and "elasticity buffer" (claim 5) must be shown or the features canceled from the claims. No new matter should be entered. In addition, the steps set forth in claim 20 must be shown in the form of a flow chart, for example.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The status of U.S. Application Serial No. 09/392,042 cited in page 12 of the originally filed specification must be updated.

Claim Rejections - 35 USC § 112

Claims 4, 5, 10, 12, and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 4, the essential structural cooperative relationships between the "phase aligner," "encoder," and "serializer" have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2172.01.

In claim 5, the essential structural cooperative relationships between the "framer," "decoder," "elasticity buffer," and "deserializer" have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2172.01.

With regard to claim 10, a description must be provided after "DC."

With regard to claim 12, "said single substrate" lacks antecedent basis.

With regard to claim 20, the "transmit channel" and "receve channel" have not been previously defined or recited in claim 17.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7, 9, 11-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Dodd et al. (6,530,006).

At the outset, it is noted that similar claims will be grouped together to avoid repetition.

As broadly drafted, these claims do not define any structure that differs from Dodd et al. (Dodd).

With regard to claim 1, Dodd discloses a high speed serial memory interface system comprising: an information configuration core (120) for coordinating proper alignment of information communication signals; a system interface (memory controller 110/120 interface) for communicating with a system controller (110), said system interface coupled to said information configuration core (120); and a memory array interface (120/memory array interface) for communicating with a memory array (130/135 or 1-8), said memory array interface coupled to said information core (120).

With regard to claim 2, the system interface of Dodd comprises: a serial read data port (it is clear that the data buffers 123/124 must include read data port for communication with the read information from controller 110) for communicating serial read information from said system controller, said serial read data port communicates said serial read information in accordance with a first synchronized clock signal (the clock for controller 110); a serial write data port (it is clear that the data buffers 123/124 must include write data port for communication with the write information from controller 110) for communicating serial write information from said system controller (110), said serial write data port communicates said serial write information in accordance with said

first synchronized clock signal (clock for controller 110); and a serial address data port (it is clear that the data buffers 123/124 must include write data port for communication with the address information from controller 110) for communicating serial address information from said system controller (110), said serial address data port communicates said serial address information in accordance with said first synchronized clock signal (clock for controller 110).

With regard to claim 3, the memory array interface of Dodd comprises: a parallel transmit port (it is clear that the buffers 123/124 must include a parallel transmit port, see additionally Fig. 5, see also col. 2, lines 54-63) for transmitting information to said memory array (1-8, for example), said parallel transmit port transmits said information in accordance with a second synchronized clock signal (clock for memory devices 130/135 or 1-8); a parallel receive port for receiving information from said memory array (it is clear that the buffers 123/124 must include a parallel receive port, see additionally Fig. 5, see also col. 2, lines 54-63), said parallel receive port receives said information in accordance with a second synchronized clock signal (clock for memory devices 130/135 or 1-8); a parallel address port (it is clear that the buffers 123/124 must include a parallel address port, see additionally Fig. 5, see also col. 2, lines 54-63) for communicating address information to an address array, said parallel address port communicates said address information in accordance with a second synchronized clock signal (clock for memory devices 130/135 or 1-8); and a control port (for communicating control information to said memory array, said control port (it is clear that the buffers 123/124 must include a control port, see additionally Fig. 5, see also col.

2, lines 54-63) communicates said control information in accordance with a second synchronized clock signal (clock for memory devices 130/135 or 1-8).

With regard to claim 4, it is clear that in the interface system of Dodd, the information configuration core (120) includes a transmit channel comprising: a phase aligner (circuit 300) for aligning signals forwarded from said memory array interface. It is also clear that the interface system of Dodd, as in any memory system interface, must include an encoder so that it can format the data. It is also clear that signals received from the memory devices 130/135 or 1-8 must be serialized. See discussion above regarding claims 2 and 3.

With regard to claim 5, since serial data is converted to parallel data (see discussion regarding to claims 2 and 3), it is clear that the serial data must be deserialized. As in any conventional memory system, a frame is a set of data stored in the buffer. It is clear that a set of data from the controller must be framed in order to store in the buffer. Since the encoder is needed from one end (see discussion regarding to claim 4), it is clear that a decoder is also needed the other end. Also, it is clear that the buffer of Dodd is a elasticity buffer. By definition, elasticity buffer connected to an oscillator is used to compensate for difference between transmitting and receiving clocks. The buffer of Dodd is used to compensate the difference in clock speed, and is connected to an oscillator 430 of circuit 300.

With regard to claims 6 and 9, it is clear that the memory clock is slower than the controller clock.

With regard to claim 7, note address and control/command buses and data buses to and from memory devices (130/135 or 1-8).

With regard to claims 11, 12, and 16, see discussion above. Note also that Dodd additionally disclose a "single chip memory module integrated high speed interface system." See at least Fig. 5 and description thereof.

With regard to claims 13 and 14, the alleged advantages are irrelevant and do not define any step/structure that differs from Dodd.

With regard to claim 15, the in any memory system, in Dodd, the data and address bits are provided synchronously upon a clock signal edge.

With regard to claims 17-20, it is clear that one using the system of Dodd would have performed the same steps set forth in claims 17-19.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dodd.

Dodd, as discussed above, discloses the claimed invention except for the use of DDR (double data rate) or "double data rated clocking." However, DDR clocking is old and well-known for its use to send data synchronously with the clock pulse signal using the double-data-rate method (DDR); wherein data transfer occurs during both the rising

and the falling edges of the clock pulse. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use DDR clocking, since the Examiner takes Official Notice that the use of DDR method is old and well-known and providing DDR clocking to Dodd only involves ordinary skill in the art. If Applicant chooses to properly challenge the Official Notice, supportive document(s) will be provided upon request.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dodd.

Dodd, as discussed above, discloses the claimed invention except for the use of a 8B/10B encoder. However, 8B/10B encoder is old and well-known for its use in serial data transmission standards to make sure there are enough transitions in the serial data stream so the clock can be recovered easily. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use 8b/10b encoder, since the Examiner takes Official Notice that the use 8B/10B encoder is old and well-known and providing 8B/10B encoder to Dodd only involves ordinary skill in the art. If Applicant chooses to properly challenge the Official Notice, supportive document(s) will be provided upon request.

U.S. Patent Nos. 6,215,727 to Parson et al., 6,493,250 to Halbert et al., 6,449,213 to Dodd et al., 6,378,018 to Tsern et al., 4,513,374 to Hooks, Jr., 6,373,302 to Li et al., and 6,502,161 to Perego et al. are cited as relevant art.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 703-308-0211.

Khanh Dang
Primary Examiner